IN THE CLAIMS

1-23. Canceled

24. (Previously Presented) A semiconductor component comprising:

a stack of semiconductor chips, the semiconductor chips being arranged in a manner fixed cohesively one on top of another, the semiconductor chips each comprising a top side and a rear side with edge sides extending there between and having contact areas extending as far as the edge sides of the semiconductor chips, the contact areas having regions accessible from both the top side and the edge sides of the semiconductor chips; and

conductor portions extending from at least one upper edge to a lower edge of the edge sides of the semiconductor chips and electrically connecting the contact areas of the semiconductor chips of the semiconductor chip stack via at least the regions of the contact areas accessible from the edge sides of the semiconductor chips.

25. (Previously Presented) The semiconductor component as claimed in claim 24, comprising the semiconductor chips having two or more different chip sizes.

26. (Previously Presented) The semiconductor component as claimed in claim 24, comprising the semiconductor chips having a different number of contact areas at their edges.

27. (Previously Presented) The semiconductor component as claimed in claim 24, wherein the contact areas are arranged on one or more of the semiconductor edge sides, the semiconductor top side, andthe semiconductor rear side so as to enable a freely selectable stacking order for the semiconductor chips forming the stack.

28. The semiconductor component as claimed in claim 24, comprising where the conductor portions comprise an adherent plastic resist which is filled with metallic nanoparticles and is electrically conductive.

29. (Previously Presented) The semiconductor component as claimed in claim 28, comprising were the nanoparticle-filled plastic resist is soluble in a solvent.

30. (Previously Presented) The semiconductor component as claimed in claim 24, comprising where the nanoparticle-filled plastic resist is patterned by laser removal.

31. (Previously Presented) The semiconductor component as claimed in claim 24, comprising where the nanoparticle-filled plastic resist is patterned photolithographically.

32. (Previously Presented) The semiconductor component as claimed in claim 24, comprising where the semiconductor chip stack comprises a multilayer rewiring layer comprising nanoparticle-filled electrically conductive patterned plastic resist layers and insulation layers arranged in between on the edge sides of the semiconductor chips.

33. (Previously Presented) A method for producing a semiconductor component comprising a stack of semiconductor chips, the method comprising:

producing semiconductor chips with contact areas extending as far as the edges of the semiconductor chip;

cohesively fixing the semiconductor chips one above another to form a semiconductor stack;

encapsulating the semiconductor stack with a layer made of a plastic resist which is filled with nanoparticles; and

patterning the layer to form interconnect sections between the contact areas of the semiconductor chips stacked one on top of another.

34. (Previously Presented) The method as claimed in claim 33, comprising spraying on the layer made of plastic resist for encapsulating the semiconductor stack.

35. (Previously Presented) The method as claimed in claim 33, comprising dipping the semiconductor stack, for encapsulation with a layer made of plastic resist, into a bath of nanoparticle-filled plastic resist.

36. (Previously Presented) The method as claimed in claim 33, comprising effecting a laser removal method for patterning the nanoparticle-filled plastic resist to form interconnect sections.

37. (Previously Presented) The method as claimed in claim 33, comprising carrying out a photolithography method for patterning the nanoparticle-filled layer made of plastic resist to form interconnect sections.

38. (Previously Presented) The method as claimed in claim 33, comprising applying the interconnect sections to the semiconductor stack selectively by precision injection techniques.

39. (Previously Presented) The method as claimed in claim 33, comprising applying multilayer interconnect sections in alternation with insulation layers to the semiconductor stack.

40. (Previously Presented) A semiconductor component comprising:

a stack of semiconductor chips, the semiconductor chips being arranged in a manner fixed cohesively one on top of another, the semiconductor chips each comprising a top side and a rear side with edge sides extending there between and having contact areas extending as far as the edge sides of the semiconductor chips, the contact areas having regions accessible from both the top side and the edge sides of the semiconductor chips;

conductor portions extending from at least one upper edge to a lower edge of the edge sides of the semiconductor chips and electrically connecting the contact areas of the semiconductor chips of the semiconductor chip stack via at least the regions of the contact areas accessible from the edge sides of the semiconductor chips;

where the electrically conductive conductor portions are arranged adhesively on the semiconductor chip edges, the semiconductor edge sides, the semiconductor top side and/or the semiconductor rear side with a freely selectable stacking order; and

where the conductor portions comprise an adherent plastic resist which is filled with metallic nanoparticles and is electrically conductive.

41. (Previously Presented) The semiconductor component as claimed in claim 40, comprising were the nanoparticle-filled plastic resist is soluble in a solvent.

42. (Previously Presented) The semiconductor component as claimed in claim 40, comprising where the nanoparticle-filled plastic resist is patterned by laser removal.

43. (Previously Presented) The semiconductor component as claimed in claim 40, comprising where the nanoparticle-filled plastic resist is patterned photolithographically.

44. (Previously Presented) The semiconductor component as claimed in claim 40, comprising where the semiconductor chip stack comprises a multilayer rewiring layer comprising nanoparticle-filled electrically conductive patterned plastic resist layers and insulation layers arranged in between on the edge sides of the semiconductor chips.

45. (Previously Presented) The semiconductor component as claimed in claim 44, comprising the semiconductor chips having two or more different chip sizes; and having a different number of contact areas at their edges.

46. (Cancelled)